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LANGHAMMER, L.; ŠOTNER, R.

Proceedings of the 2020 30th International Conference Radioelektronika, pp. 1-4

eISBN: 978-1-7281-6469-4

DOI: <https://doi.org/10.1109/RADIOELEKTRONIKA49387.2020.9092421>

Accepted manuscript

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DOI: 10.1109/RADIOELEKTRONIKA49387.2020.9092421. Final version is available at <https://ieeexplore.ieee.org/document/9092421>

Conversion of a MISO Filter into its Reconnection-less Reconfigurable Form with Complex Active elements

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Abstract—This paper aims to show an easy way how to design a reconnection-less reconfigurable filter based on the modification of an existing MISO filter. The proposed filter offers the same transfer functions as the structure before the modification and additionally offers function of the direct transfer and high-pass function with transfer zero. In comparison with the structure before the modification, the proposed filter provides the electronic control of its pole frequency and quality factor. The design is supported by simulations in Cadence IC6 (spectre).

Keywords—electronic reconfiguration, frequency filter, MISO filter, reconnection-less reconfiguration, VDCC

I. INTRODUCTION

The development of the electronic industry and the signal processing creates increasing demands on all type of circuitry including the frequency filters. A feature of frequency filters to be more and more versatile (provide multiple types of the transfer function of given filtering structure) is a common trend of the last decade. The possibility to provide all standard filtering functions (high-pass (HP), low-pass (LP), band-pass (BP), band-stop (BP) and all-pass (AP) functions) can be quite beneficial so we can use whichever function is currently demanded. One of the typical types of filtering structures, which are designed to offer multiple diverse transfer functions, is so called Multiple-Input Single-Output (MISO) filter. These filters [1-11], as the name suggests, consist of multiple input terminals and single output terminal where the resulting output response is given by specific selection or the particular combination of the excitation voltage(s) or current(s) used at that moment. As a result, it suggests the usage of copies of the input voltage/current or even their increased (multiplied) or decreased value in some cases. The fact, we might need multiple input signal copies or their increased/decreased value applied to different circuit nodes, can become increasingly technically difficult. It also brings other possible issues with the required logic/mechanism for switching between different inputs/excitation nodes of the given filtering structure (overshoots and possible distortion of the signal caused by the switching mechanism).

The mentioned issues can be solved by the utilization of reconnection-less reconfigurable filters [12-16]. These filters can be understood as a two-port structure (having one input and one output). The output response is then changed solely in electronic manner without manual modification of the circuit topology or a position of input or output port(s). The design of the reconnection-less reconfigurable filters can

be approached by two conventional means. The first one is to purposely design a filter with the ability of the reconnection-less reconfiguration in mind right from the beginning of the design procedure [12-15]. The other approach is based on the suitable modification of an existing structure which does not possess the such ability [16].

The proposal in this paper is using the second mentioned approach in order to show a simple way how obtain the reconnection-less reconfigurable ability from a standard MISO filter. The designed filter offers all standard 2nd-order transfer functions from the same topology without any necessary modification of the structure or switching between nodes. The filter is operating in the current mode (having current input and current output) which offers possible advantages such as lower power consumption better signal-to-noise ratio and wider bandwidth operational range, in particular cases [17].

II. PREVIOUSLY PROPOSED MISO FILTER

The structure, used for the purposes of the design of the reconnection-less reconfigurable filter based on the modification of an existing circuit, is a MISO filter presented in [18]. The core of the filter is created by one voltage differencing current conveyor (VDCC). The behavior of the VDCC can be expressed by the following relations $I_Z = g_m(V_P - V_N)$, $V_X = V_Z$, $I_{Wp} = I_X$ and $I_{Wn} = -I_X$. This element has four high impedance terminals (P, N, Z, W) and one low impedance terminal (X). Fig. 1 a) depicts the schematic symbol of the VDTA and Fig. 1 b) then introduces its internal structure created by one operational transconductance amplifier (OTA) and one second-generation current conveyor (CCII).

The filter from [18] (see Fig. 2) offers LP, BP, HP, BS and AP transfer functions and has three inputs when a manual reconnection of particular input, their suitable combination, or the necessity of the multiplied value of the input current is required in order to obtain all available transfer functions. The structure in Fig. 2 is consisting of one VDCC, two capacitors and a one resistor. The transfer function of the filter from Fig. 2 is expressed as $K(s)=N(s)/D(s)$, where (G stands for the conductance of resistor R):

$$N(s) = i_{IN1}sC_2G - i_{IN2}(sC_1G + g_mG) + i_{IN3}(s^2C_1C_2 + sC_1G + g_mG) \quad (1)$$

$$D(s) = s^2C_1C_2 + sC_1G + g_mG \quad (2)$$

For the research, infrastructure of the SIX Center was used.

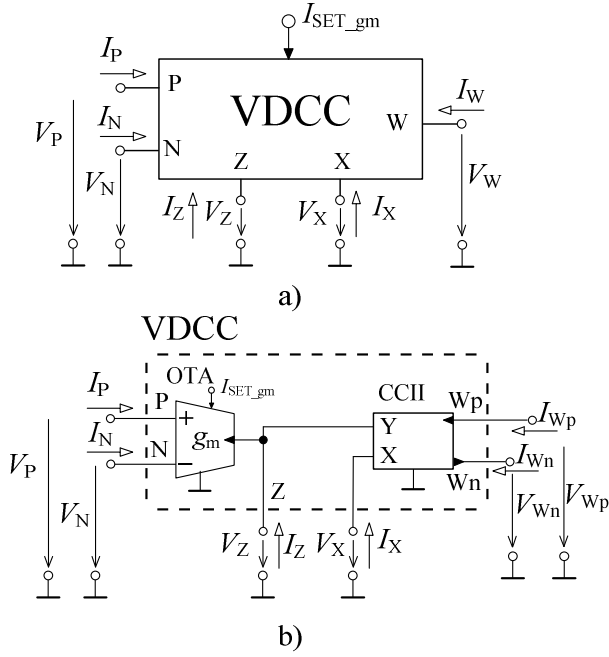


Fig. 1. Voltage Differencing Current Conveyor (VDCC): a) schematic symbol, b) its inter structure created by one OTA and one CCII.

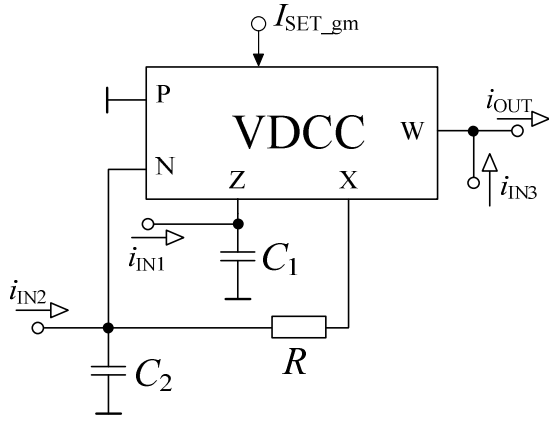


Fig. 2. MISO current-mode filter presented in [19] used for the conversion into its reconnection-less reconfigurable form.

The available output responses (all in non-inverting form) are obtained as follows:

- BP function for i_{IN1} being used, $i_{IN2} = i_{IN3} = 0$.
- LP function for i_{IN1} and i_{IN2} being used, $i_{IN3} = 0$.
- HP function for i_{IN2} and i_{IN3} being used, $i_{IN1} = 0$.
- BS function for i_{IN3} and inversion of i_{IN1} being used, $i_{IN2} = 0$.
- AP function for i_{IN3} and inversion of double value of i_{IN1} being used, $i_{IN2} = 0$.

The relations for the angular frequency ω_0 and quality factor Q are given as:

$$\omega_0 = \sqrt{\frac{g_m G}{C_1 C_2}}, \quad Q = \sqrt{\frac{C_2 g_m}{C_1 G}}. \quad (3, 4)$$

III. DESIGN PROCEDURE

In order to create a reconnection-less reconfigurable filter from the structure in Fig. 2, given structure has been complemented by a current amplifier introduced in [19] which offers the ability to control the gain of each output independently (in text referred to as individual output gain controlled current amplifier (IOGC-CA)). The schematic symbol of the IOGC-CA is presented in Fig. 3 a). The behavior of this element is given as $I_{OUT\pm} = \pm B_i I_{IN}$ where $i = \{1, 2, 3\}$.

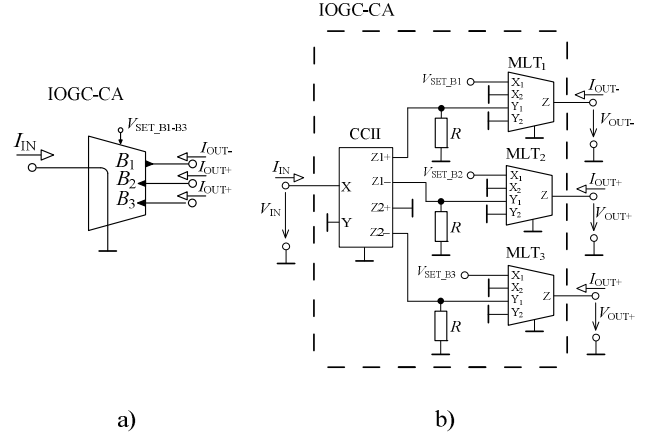


Fig. 3. Independent output gain controlled current amplifier (IOGC-CA): a) schematic symbol, b) specific implementation of its inter structure.

This modification has been done to distribute the input current and provide its multiplied or decreased value if necessary changing the filtering structure from having three inputs into a single-input single-output filter. Each original input current (i_{IN1} , i_{IN2} and i_{IN3}) can be now applied using transfers which are controlled electronically by gains B_1 , B_2 and B_3 . Consequently, this modification can change generally any MISO filter into a reconnection-less reconfigurable filter. The inter structure of the IOGC-CA (shown in Fig. 3 b)) has been created with help of a current conveyor with four outputs and multipliers presented in [20] in this particular case. Both these devices are designed in ON Semiconductor 0.35 μm I3T CMOS process. Similarly, the OTA and CCII from the inter structure of the VDCC have been created by the same devices from [20]. The current conveyor from the inter structure of the IOGC-CA offers the copies of the input current and the multipliers together with resistors provide the electronically controllable transfers of individual outputs. The current gain of an individual output of the IOGC-CA is given as follows: the current from the output of the current conveyor is transferred into voltage by the resistor R . Then, this voltage is applied to the voltage input of a multiplier and transferred back to current based on the electronically controllable transconductance g_m . Thus, the resulting output current (current gain of given output) is based on the ratio between the value of resistor R which is fixed (1 k Ω) and transconductance g_m which is controlled by the DC voltage. Therefore, the control voltage (labeled as V_{SET_B}) is adjusting the transconductance but as a result it controls the current gain as well. This solution has been made due to the lack of a suitable current amplifier simulation model implemented in the used CMOS process in our case.

Some polarities of the outputs of the active elements within the filter in Fig. 2 have been altered so the inversion of the input current is required only for one function

(formerly, the inversion was required in case of two functions (BS and AP)). As a result, LP and BS functions are now inverting. Nonetheless, this can be easily compensated since the used multiplier can provide both polarities of the output current in comparison the most of commercially available devices. The last modification involves the removal of the resistor R in the filtering structure since the used current conveyor has an electronically controlled intrinsic resistance of its X input R_X . Except of the fact this step will decrease the number of passive elements within the filter, it will also enable the electronic control of the pole frequency f_0 and quality factor Q (g_m is controlled by V_{SET_gm} , originally was controlled by I_{SET_gm} , R_X is controlled by I_{SET_RX}) which were controlled by the change of the transconductance g_m but also the change of the value of the resistor R . The resulting structure of the proposed reconnection-less reconfigurable filter is shown in Fig. 4. The circuit involves one VDCC, one IOGC-CA and two grounded capacitors.

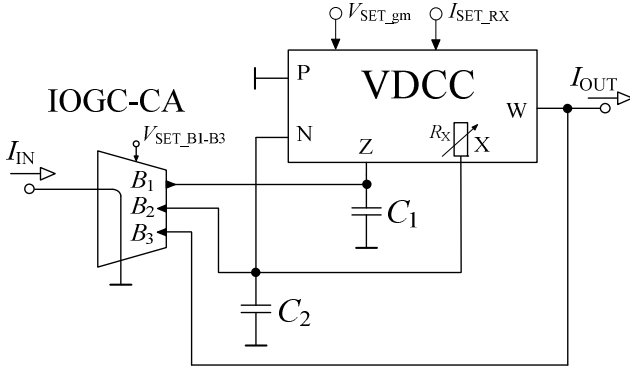


Fig. 4. Proposed reconnection-less reconfigurable filter created from the MISO filter from [19].

The transfer function of the filter in Fig. 4 is expressed as $K(s)=N(s)/D(s)$ where (G_X is equal to $1/R_X$):

$$N(s) = -B_1 s C_2 G_X + B_2 (-s C_1 G_X + g_m G_X) + B_3 (s^2 C_1 C_2 + s C_1 G_X + g_m G_X) \quad (5)$$

$$D(s) = s^2 C_1 C_2 + s C_1 G_X + g_m G_X \quad (6)$$

The angular frequency ω_0 and quality factor Q are given by:

$$\omega_0 = \sqrt{\frac{g_m G_X}{C_1 C_2}}, \quad Q = \sqrt{\frac{C_2 g_m}{C_1 G_X}} \quad (7, 8)$$

The available output responses are based on the following setting (except for already mentioned functions, it is also possible to obtain direct transfer (DT) and HP function with transfer zero (HPZ)):

- BP function for $B_1 = 1, B_2 = B_3 = 0$.
- LP function for $B_1 = -1, B_2 = 1, B_3 = 0$.
- HP function for $B_2 = B_3 = 1, B_1 = 0$.
- BS function for $B_1 = B_3 = 1, B_2 = 0$.
- AP function for $B_1 = 2, B_3 = 1, B_2 = 0$.

- DT function for $B_1 = B_2 = 0, B_3 = 1$.
- HPZ function for $B_1 > 0, B_2 > 0, B_3 = 1, B_1 + B_2 = 1$.

For the used implementation, current gain $B = 1$ is obtained for $V_{SET_B} = 0.5$ V, $B = 0$ is for $V_{SET_B} = 0$ V and $B = 2$ for $V_{SET_B} = 1$ V.

IV. SIMULATION RESULTS

The design has been verified my simulations in Cadence IC6 (spectre) with help of simulation models of available active elements based on ON Semiconductor 0.35 μ m I3T CMOS process. Specific implementation of used active elements is described in section II and III. The numerical design for the simulation has following specification: capacitors $C_1 = C_2 = 820$ pF, the value of transconductance g_m is set to 1 mS and the value of intrinsic resistance R_X is equal to 1 k Ω . Based on these values, the theoretical f_0 and Q are determined to be $f_0 = 194.1$ kHz and $Q = 1$. Current gains B are depending on particular output function (the setting is given in the previous section). The power consumption of the proposed structure was 70.4 mW.

The characteristics of all standard 2nd-order transfer functions are presented in Fig 5 and Fig 6. Magnitude and phase characteristics of available functions of BP (blue lines), LP (red lines), HP (green lines) and BS (teal lines) obtained from simulations are compared with the theoretical expectations (black dashed lines) in Fig. 5 a), b), respectively. Figure 6 shows the magnitude (green line), phase (red line) and group delay (blue line) of AP filter again compared with the theoretical characteristics (black dashed lines). Eventual deviations of all results from the theory are the product of parasitic characteristics of utilized simulation models.

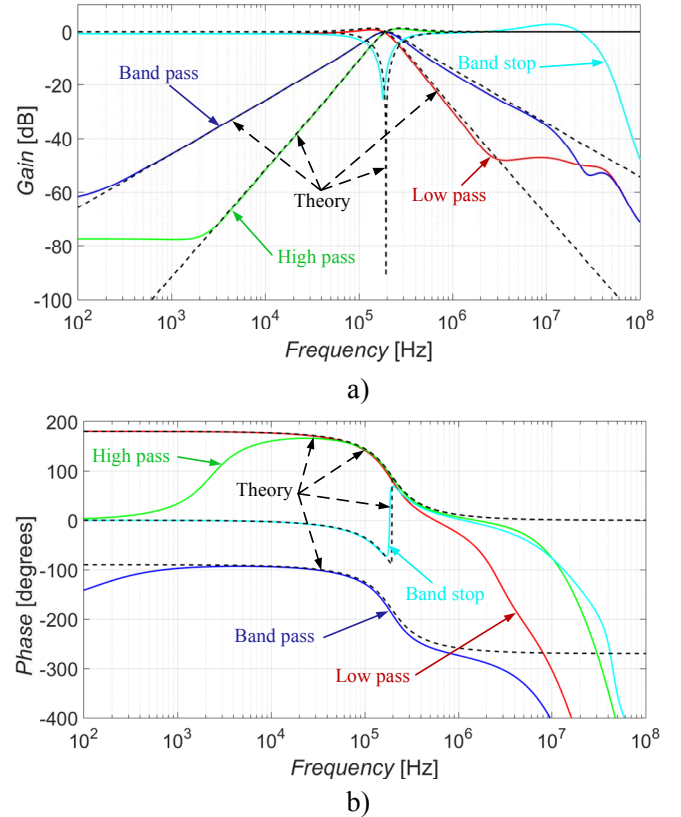


Fig. 5. Comparison of simulated and theoretical functions of BP, LP, HP and BS: a) magnitude characteristics, b) phase characteristics.

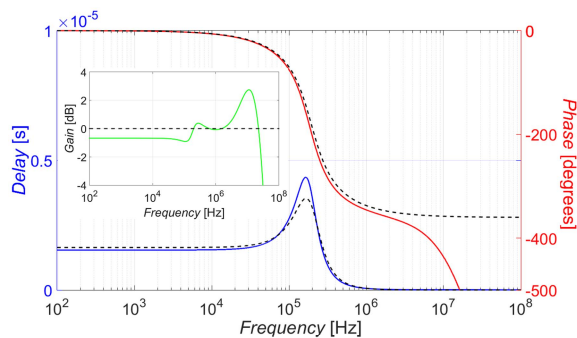


Fig. 6. Comparison of simulated and theoretical characteristics (magnitude, phase and group delay) of the AP filter.

Figure 7 shows how the output response can be changed in accordance to the setting of current gains B_1 to B_3 . It can be seen that we can come from HP function ($B_1 = 0, B_2 = 1, B_3 = 1$) over HPZ function ($B_1 = 0.01, B_2 = 0.99, B_3 = 1$ and $B_1 = 0.1, B_2 = 0.9, B_3 = 1$) to BP function ($B_1 = 1, B_2 = 0, B_3 = 1$) all by simple change of the electronically controllable parameters without any manual modification of the filtering structure.

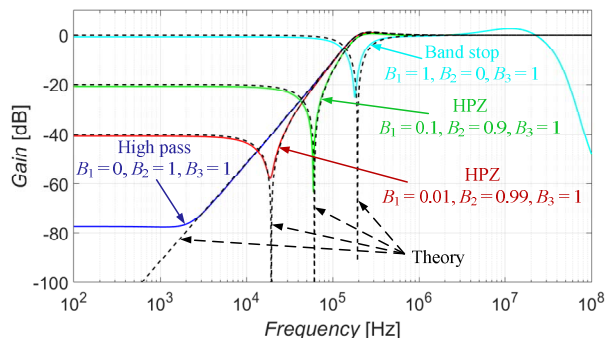


Fig. 7. Comparison of simulated and theoretical characteristics (magnitude, phase and group delay) of the AP filter.

V. CONCLUSION

The modification of given MISO filter, except for the feature of the reconnection-less reconfiguration, also brings two additional available transfer functions (DT and HPZ) and the ability of the electronic control of the pole frequency and quality factor, in this particular case. The resulting functions can be easily fine-tuned thanks to analog (continuous) control of individual current gains. Cadence simulations support the design and show good agreement of simulation results with the theoretical expectations.

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